WHAT IS CLAIMED IS:

1. A thin film transistor substrate for a liquid crystal display, comprising:

a source electrode connected to a data line so as to receive video data;

a drain electrode opposed to the source electrode;

a channel between the drain electrode and the source electrode, wherein the channel has a desired size; and

a gate electrode for opening and closing the channel, wherein the gate electrode includes a head portion having at least one side inclined at a predetermined angle.

2. The thin film transistor substrate as claimed in claim 1, wherein the head is inclined parallel to a rubbing direction.

3. The thin film transistor substrate as claimed in claim 1, wherein the head is inclined between about 35° to 45° from the longitudinal direction of the gate electrode.

4. The thin film transistor substrate as claimed in claim 1, wherein the gate electrode includes a concave neck, and wherein the concave neck reduces overlap of the drain electrode and the gate electrode.

5. The thin film transistor substrate as claimed in claim 4, wherein the neck is narrower than a maximum width of the head by less than about 5μm.

6. The thin film transistor substrate as claimed in claim 1, further comprising:

a gate insulating film on the substrate and over the gate electrode;

a semiconductor layer on the gate insulating film and over the gate electrode;

a protective layer over the gate insulating film and over the source and drain electrodes; and

a pixel electrode on the protective layer and connected to the drain electrode;

wherein the source and drain electrodes are on the semiconductor layer.

7. The thin film transistor substrate as claimed in claim 6, wherein the pixel electrode is formed with an edge that follows the inclination of the head, and wherein the pixel electrode further corresponds with the neck of the gate electrode.

8. The thin film transistor substrate as claimed in claim 1, further comprising:

a gate insulating film on the substrate and gate electrode;

an active layer and an ohmic contact layer over the gate insulating film, wherein the active layer and the ohmic contact layer overlap the gate electrode;

a protective layer over the gate insulating film and patterned to match the active layer; and

a pixel electrode on the protective layer and connected to the drain electrode;

wherein the source and drain electrodes are pattern to match the ohmic contact layer;

9. The thin film transistor substrate as claimed in claim 8, wherein the pixel electrode is formed with an edge that follows the inclination of the head, and wherein the pixel electrode further corresponds with the neck of the gate electrode.

10. The thin film transistor substrate as claimed in claim 1, further comprising:

a gate insulating film on the substrate and over the gate electrode;

a semiconductor layer on the gate insulating film and over the gate electrode;

a protective layer on the gate insulating film and over the source and drain electrodes; and

a pixel electrode on the protective layer and connected to the drain electrode;

wherein the source and drain electrodes correspond with the semiconductor.

11. The thin film transistor substrate as claimed in claim 10, wherein the pixel electrode is formed with an edge that follows the inclination of the head, and wherein the pixel electrode further corresponds with the neck of the gate electrode.

12. A method of fabricating a thin film transistor substrate, comprising the steps of:

forming a gate metal layer on a substrate; and

patterning the gate metal layer to form a gate electrode having a head portion with at least one side inclined at a desired angle.

13. The method as claimed in claim 12, further comprising the steps of:

forming a gate insulating film on the substrate and over the gate electrode;

forming a semiconductor layer on the gate insulating film;

forming source and drain electrodes on the semiconductor layer so as to define a channel;

forming a protective layer on the gate insulating film and over the source and drain electrodes; and

forming a pixel electrode on the protective layer.

14. The method as claimed in claim 12, further comprising the steps of:

forming a gate insulating film on the substrate in such a manner as to cover the gate electrode;

depositing first and second semiconductor layers and a metal layer on the gate insulating film;

patterning the metal layer and the second semiconductor layer to form source and drain electrodes;

providing a protective material layer on the first semiconductor layer in such a manner as to cover the source and drain electrodes,

patterning the first semiconductor layer and the protective layer material to form a protective layer and a semiconductor pattern; and

forming a pixel electrode on the protective layer.

15. The method as claimed in claim 12, further comprising the steps of:

forming a gate insulating film and a semiconductor material on the substrate in such as a manner to cover the gate electrode;

forming source and drain electrodes on the semiconductor material;

depositing a protective layer material on the gate insulating film in such a manner as to cover the source and drain electrodes,

simultaneously patterning the semiconductor material and the protective layer material to form a semiconductor pattern and a protective layer; and

forming a pixel electrode on the protective layer.

16. The method as claimed in claim 12, further comprising the steps of forming a gate electrode having a head portion inclined parallel to a rubbing direction of the thin film transistor substrate.

17. The method as claimed in claim 16, further comprising the steps of forming a gate electrode having a neck portion that is narrower than a maximum width of the head portion by less than about 5μm.

18. The method as claimed in claim 17, further comprising the steps of:

forming a gate insulating film over the gate electrode;

forming a semiconductor layer on the gate insulating film; and

forming source and drain electrodes on the semiconductor layer so as to define a channel.

19. The method as claimed in claim 18, further comprising the steps of providing a protective material layer on the semiconductor layer.

20. The method as claimed in claim 19, further comprising the steps of forming a pixel electrode on the protective layer.